PRESS RELEASE

Powerful FPGA Design Creation and Simulation IDE Adds VHDL-2019 Support & OSVVM Enhancements

Aldec's Active-HDL™ enables FPGA designers to take full advantage of the many features within the latest revision to VHDL *and* helps improve design verification efficiency.

Henderson, NV – January 20, 2021 – Aldec, Inc., a pioneer in mixed HDL language simulation and hardware-assisted verification for FPGA and ASIC designs, has enhanced Active-HDL™ to support new features within VHDL-2019 (IEEE 1076-2019). These features simplify the language, lift certain restrictions that were present in earlier versions and introduce new application programming interfaces (APIs).

Support has also been added for release 2020.08 of the open source VHDL verification methodology (OSVVM).

Active-HDL is an integrated design environment (IDE) that includes a full HDL and graphical design tool suite plus an RTL / gate-level simulator for the rapid deployment and verification of FPGAs. These features, combined with the latest revisions to VHDL, empower engineers to create, maintain, re-use and easily verify their designs.

"VHDL-2019 was requested by users, ranked by users, scrutinized by users, written by users, and balloted by the VHDL community," comments Jim Lewis Director of VHDL Training at SynthWorks and IEEE 1076 VHDL Working Group Chair. "Just as they were for VHDL-2008, Aldec is at the forefront of implementing the new language features. This is good news as the VHDL verification community is ready to start using VHDL-2019."

Support for OSVVM 2020.08 gives users of Active-HDL access to the free and open-source methodology's new requirements tracking, updated scripting, AXI4 full verification components, and model independent transactions.

Sunil Sahoo, Aldec's SW Product Manager, adds: "We're committed to the VHDL user community from an EDA tools perspective as well as supporting all methodologies that aim to boost productivity and give engineers confidence in their designs."

The latest version of Active-HDL also sees SystemVerilog enhancements that include initial support for multidimensional arrays of instances, preliminary support of unresolved user-defined nettypes, and preliminary support for unique constraints.

Several non-standard extensions to SystemVerilog are present in the latest release of Active-HDL too. These include allowing variable type outputs of clocking blocks to be driven by a continuous assignment, allowing the use of foreach loops iterating over the elements of a subarray, and assigning a virtual interface with a modport to a virtual interface without a modport.

Active-HDL 12.0 is now available for download and evaluation.

MAIN ENDS

Aldec's Active-HDL™ enables FPGA designers to take full advantage of the many features within the latest revision to VHDL and helps improve design verification efficiency.

NOTES TO EDITORS

About VHDL-2019
(source: osvvm.org)

VHDL-2019 was approved by IEEE RevCom in September 2019 and published in December 2019. It was an effort supported mainly by VHDL users – from requirements definition to LRM writing. This is different from the past where employees of EDA vendors did much of the work – particularly the LRM writing.

Language changes were use-model-driven and had multiple opportunities to be pruned from implementation. The process started with a discussion of feature requests. Feature requests were then voted on and ranked.
High ranked features were discussed and developed into proposals. Proposals were required to provide use models to affirm their worth and validity. Proposals were then developed into language change specifications (LCS).

The entire process was driven by volunteers – and again almost all were users. Volunteerism added another level of scrutiny to the request and/or proposal. If no one was willing to write a proposal or an LCS for an item, then no matter how high the feature or proposal was ranked, it failed to be worthy of being implemented.

This revision brings many updates, such as:

- Interfaces. These allow abstract connections between designs.
- Conditional Compilation, as requested for by users many times.
- Protected Type Enhancements. These allow VHDL verification libraries, such as OSVVM, to further improve verification capabilities. *VHDL can do verification? YES! As a verification library, OSVVM provides similar capabilities to SystemVerilog+UVM and in the European FPGA market OSVVM is used more than SystemVerilog+UVM.*
- Shared Variables on Entity Interfaces. This allows verification data structures, such as the OSVVM generic scoreboard, to be passed into a verification component.
- API for Assert and PSL information. This allows for reporting the number of Assert WARNING, ERROR, and FAILURE messages that occur in a simulation. Similarly, the API for PSL gives us error and coverage seen by PSL. Couple these together with the error reporting capability of OSVVM and we can generate a detailed pass/fail report for a simulation.
- API for Calling Path Information. This allows subprograms to provide detailed trace back information on the source of an error.
- Generic Type Enhancements. These allow us to create better generic packages for verification and RTL usage.
- 64 Bit Integers64-bit integers. The community has been asking for larger integers. Moving to 64 bits is seen as a first step toward a longer-term solution.
- Conditional Expressions. These allow for the use of conditionals like “when else” in contexts such as declarations.
- API to access Date, Time and File System. This API simplifies the process to create a design build register.

About Active-HDL

Active-HDL™ is a Windows® based, integrated FPGA Design Creation and Simulation solution for team-based environments. Active-HDL’s Integrated Design Environment (IDE) includes a full HDL and graphical design tool suite and RTL/gate-level mixed-language simulator for rapid deployment and verification of FPGA designs.

About Aldec

Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, CDC Verification, IP Cores, High-Performance Computing Platforms, Embedded Development Systems, Requirements Lifecycle Management, DO-254 Functional Verification and Military/Aerospace solutions. www.aldec.com

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Media Contact:
Richard Warrilow
Declaration Limited
T: +44 (0)1522 789 000
richardw@aldec.com