PRESS RELEASE

Riviera-PRO™: OSVVM 2020.08 inclusion, enhanced language support, and new debugging features aim to boost productivity

Henderson, NV – December 8, 2020 – Aldec, Inc., a pioneer in mixed HDL language simulation and hardware-assisted verification for FPGA and ASIC designs, has updated Riviera-PRO™ to include the 2020.08 revision of the open-source VHDL verification methodology (OSVVM). This gives users of Aldec's popular simulation platform access to OSVVM's new requirements tracking, updated scripting, AXI4 full verification components, and model independent transactions.

The latest version of Riviera-PRO (release 2020.10) also includes SystemVerilog and VHDL-2019 simulation enhancements. For SystemVerilog, the enhancements include extended support for 4-state integral packed unions, 2-state integral packed vectors, structures and unions, and fixed-size unpacked vectors, structures and unions. For VHDL-2019, the enhancements include support for arrays and records of protected types.

"In terms of VHDL-2019 support, Aldec is well ahead of the game," comments Jim Lewis Director of VHDL Training at SynthWorks and IEEE 1076 VHDL Working Group Chair. "The company's Riviera-PRO introduced several VHDL-2019 support features back in June 2020, and the enhancements announced today will facilitate the development of advanced verification capabilities."

Sunil Sahoo, Aldec's SW Product Manager, adds: "Aldec is committed to keeping Riviera-PRO a powerful simulation platform in its own right, and all enhancements introduced in any given release are in direct response to requests and suggestions from engineers. We're also committed to the VHDL community and believe we currently provide more VHDL-2019 support than any other vendor."

Debugging and performance enhancements are present in Riviera-PRO release 2020.10 too. These include support for new coverage pragmas within the Verilog compiler, randomization performance enhancements (for specific cases of random constraints) and an increase to the speed at which models are drawn into Riviera-PRO's UVM Graph window.

Riviera-PRO 2020.10 is now available for download and evaluation.

MAIN ENDS

Notes to Editors

About Riviera-PRO™

Riviera-PRO™ addresses verification needs of engineers crafting tomorrow's cutting-edge FPGA and SoC devices. The tool enables the ultimate testbench productivity, reusability, and automation by combining the high-performance simulation engine, advanced debugging capabilities at different levels of abstraction, and support for the latest Language and Verification Library Standards.

About Aldec

Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, CDC Verification, IP Cores, High-Performance Computing Platforms, Embedded Development Systems, Requirements Lifecycle Management, DO-254 Functional Verification and Military/Aerospace solutions. www.aldec.com

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