PRESS RELEASE

Riviera-PRO™ Enables VHDL-2019 Users to Unleash the Power of the Language's New Additions

Henderson, NV – May 18, 2021 – Aldec, Inc., a pioneer in mixed HDL language simulation and hardware-assisted verification for FPGA and ASIC designs, provides industry's most comprehensive implementation of VHDL 2019 for both Windows and Linux platforms with the latest release of Riviera-PRO (release version 2021.04).

One of the most important features now supported is Interfaces. These have historically been difficult to model in VHDL. In VHDL-2019 (a.k.a. IEEE 1076-2019), they are accommodated using a record and a mode view. Along with other new features, Interfaces enable users to create code that is more compact and more reusable.

VHDL-2019 simulation features added to Riviera-PRO include support for arrays and records of the file type, the introduction of sequential block statements, and the *STD* library has been enhanced with the *REFLECTION* package.

"The improved support of Interfaces to VHDL was one of the most exciting in the VHDL-2019 release, and their implementation was the direct result of requests from the VHDL user community, which put forward usage models to justify the addition," comments Sunil Sahoo, Riviera-PRO Product Manager. "We also listen to the community. When launching or enhancing our EDA tools, Aldec always does so in direct response to our users' needs and requests, and the improved support of Interfaces builds on an early provision for VHDL-2019 we introduced in Riviera-PRO last year. Most other EDA tool vendors have yet to cater for VHDL-2019 in any way."

Riviera-PRO has also received a variety of SystemVerilog simulation enhancements. These include: the data type of a user-defined *nettype* can be specified with a type parameter, and *randomsequence* statements can now be declared in modules and classes parameterized by a type.

Riviera-PRO 2021.04 for Windows or Linux is now available for download and evaluation.

MAIN ENDS

Notes to Editors

About Riviera-PRO™

Riviera-PRO™ addresses verification needs of engineers crafting tomorrow's cutting-edge FPGA and SoC devices. The tool enables the ultimate testbench productivity, reusability, and automation by combining the high-performance simulation engine, advanced debugging capabilities at different levels of abstraction, and support for the latest Language and Verification Library Standards.

About Aldec

Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, CDC Verification, IP Cores, High-Performance Computing Platforms, Embedded Development Systems, Requirements Lifecycle Management, DO-254 Functional Verification and Military/Aerospace solutions. www.aldec.com

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Media Contact:

Richard Warrilow

Declaration Limited

T: +44 (0)1522 789 000

richardw@aldec.com