



**PRESS RELEASE**

## **New HES Board is Ideal for Prototyping and Emulating Medium to Large ASIC & SoC Designs**

**Henderson, NV, USA – July 19, 2021** – Aldec, Inc., a pioneer in mixed HDL language simulation and hardware-assisted verification for FPGA and ASIC designs, has launched the HES-VU19PD-ZU7EV, an ASIC/SoC physical prototyping and hardware emulation board that can accommodate designs of about 83M ASIC gates in size.

Compared to boards of a similar capacity, the HES-VU19PD-ZU7EV uses just two FPGAs for the provision of logic. This simplifies FPGA partitioning and reduces project bring-up time for designs targeting a medium-sized ASIC or SoC. For larger designs, four boards can be connected via a high-speed backplane (scheduled for launch later in the year) to provide the equivalent of about 332M ASIC gates. It will also be possible to connect backplanes together (up to three), to cater for designs of about 996M ASIC gates.

The HES-VU19PD-ZU7EV's logic module FPGAs are both Virtex UltraScale+ VU19P devices, Xilinx's highest logic capacity FPGA to date. Aldec's new HES board also features a Xilinx Zynq UltraScale+ ZU7EV MPSoC. It acts as the host module and has a quad-core ARM Cortex-A53, dual-core ARM Cortex-R5 real-time processing units and PCIe Gen3 embedded IP.

*"Our latest Virtex UltraScale+ VU19P device is naturally geared for ASIC and SoC prototyping," said Chris Stinson, senior director of Test, Measurement and Emulation Markets at Xilinx. "Aldec's inclusion of two of these devices, along with one of our most powerful Zynq FPGAs, has resulted in an extremely versatile platform that will enable designers to fast-track their ASIC and SoC projects."*

Zibi Zalewski, General Manager of Aldec's Hardware Division, comments: *"For this new platform we've replicated much of the system architecture of our popular dual FPGA boards in our HES-7 family and incorporated the newest and largest UltraScale+ FPGAs from Xilinx to greatly extend the*

*capacity and functionality for both emulation and prototyping scenarios. Also, our use of the Zynq US+ device as a controller, means it can host the testbench for prototyping. Indeed, the prototyping and emulation capabilities of our HES boards is unique to Aldec.”*

Zalewski goes on to indicate that a revision to HES-DVM, Aldec’s fully automated and scalable hybrid verification environment for SoC and ASIC designs, is in the pipeline. He adds: *“That will further unleash the power of the new board, through enhanced debug capabilities, for example.”*

HES-VU19PD-7U7EV has a PCIe Switch device which provides PCIe x16 Gen 3 connections with the logic devices and PCIe x8 Gen 3 connections with the controller FPGA. Other interfaces include QSFP-DD on each of the logic FPGAs and Ethernet (1Gb) and USB on the control FPGA.

In terms of interfacing with memory, the new HES board provides five SODIMMs for accommodating external DDR4 memory (two per VU19P and one for the ZU7EV) plus NVMe M.2 PCIe for additional SSD storage.

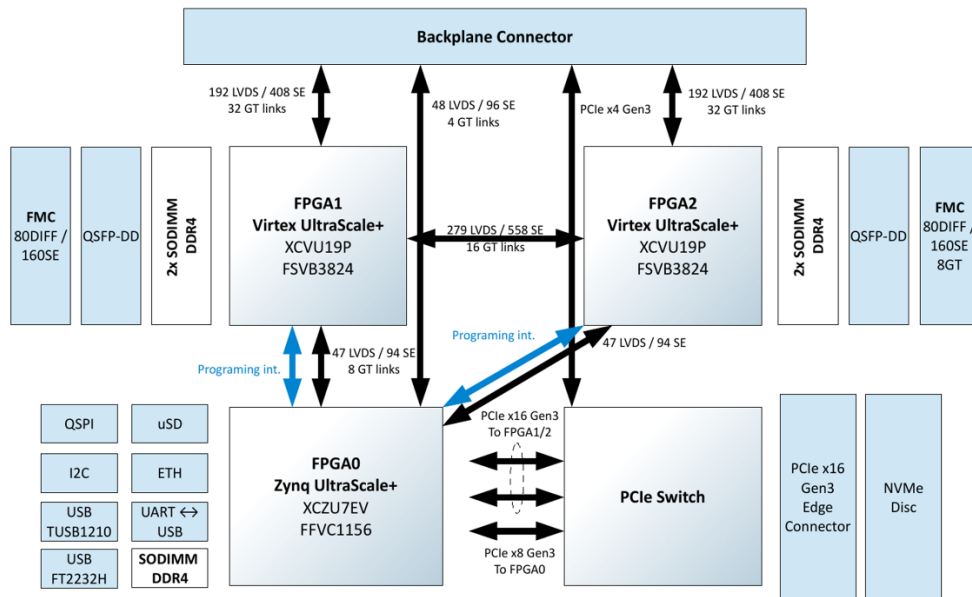
HES-VU19PD-7U7EV is supplied with Aldec’s HES Proto-AXI software package which includes all necessary drivers and utilities for communicating with and programming the board. For quick bring-up of the host connection, Aldec provides a ready-to-use image of the embedded Linux for the ZU7EV device.

*A HES Proto-AXI solution is available as an optional extra. Part of Proto-AXI Installer package, it comes with technical documentation and design examples.*

The new board also features two FMC connectors for interfacing with daughter cards to greatly assist in the development of SoCs for use in a wide range of applications.

The HES-VU19PD-7U7EV is sampling now with full production scheduled for early Q3. Full product details are available [here](#).

MAIN ENDS



*Above, the architecture of Aldec's HES-VU19PD-ZU7EV, an ASIC/SoC physical prototyping and hardware emulation board that can accommodate designs of about 83M ASIC gates in size.*

### About HES™ Prototyping Boards

HES™ is a feature-rich family of SoC/ASIC pre-silicon physical prototyping and hardware emulation boards. The family features boards with high-performance devices from either Xilinx (including Virtex-7, Virtex UltraScale, Virtex UltraScale+ and Zynq UltraScale+) or Microchip (PolarFire and SmartFusion2).

HES high-speed backplanes means boards can be interconnected and designs targeting ASICs or SoCs of several 100m ASIC gates can be easily accommodated. In addition, all boards can be used with Aldec's range of FMC daughter cards, the widest range in the EDA industry. HES boards can also be used for algorithm acceleration in High-Performance Computing (HPC) applications, such as High-Frequency Trading (HFT), computer vision and genome alignment.

### About HES-DVM

HES-DVM™ is a fully automated and scalable hybrid verification environment for SoC and ASIC designs. Utilizing the latest co-emulation standards like SCE-MI or TLM and newest FPGA technology, hardware and software design teams obtain early access to the hardware prototype of the design. Working concurrently with one another they can develop and verify high-level code with RTL accuracy and speed-effective SoC emulation or prototyping models reducing test time and a risk of silicon re-spins.

## **About Aldec**

Aldec Inc., headquartered in Henderson, Nevada, is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, CDC Verification, IP Cores, Requirements Lifecycle Management, DO-254 Functional Verification and Military/Aerospace solutions. [www.aldec.com](http://www.aldec.com)

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Media Contact:

**Richard Warrilow**

**Declaration Limited**

**T: +44 (0)1522 789 000**

**[richardw@aldec.com](mailto:richardw@aldec.com)**